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09/699,019	10/27/2000	Ahmadreza Rofougaran	40883/CAG/B600	5832
7590 03/21/2007 CHRISTOPHER C. WINSLADE McANDREWS, HELD & MALLOY 500 W. MADISON STREET SUITE 3400 CHICAGO, IL 60661			EXAMINER MILORD, MARCEAU	
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			2618	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 09/699,019	<b>Applicant(s)</b> A.ROFOUGARAN	
	<b>Examiner</b> Marceau Milord	<b>Art Unit</b> 2618	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 January 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-66 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 12, 13, 20-35 and 54-66 is/are rejected.
- 7) ☒ Claim(s) 2-11, 14-19, 36-45 and 47-53 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 12-13, 31-35, 46, 54-66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coppola (US Patent No 6020783) in view of Yu et al (US Patent No 6804359 B1).

Regarding claim 1, Coppola discloses a notch filter (fig. 1 and fig. 3), comprising: a first filter (15 of fig. 1) to output a plurality of phases of an input signal including a first phase and an inverted first phase (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52); and a second filter (21 of fig. 1) having an input to receive the inverted first phase and an inverted input to receive the first phase (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

However, Coppola does not specifically disclose that the first and second filters are polyphase filters.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Regarding claims 12-13, Coppola discloses a notch filter (fig. 1), comprising: a first filter (15 of fig. 1) including an input, and an output having a non-inverted output and an inverted output 22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52); and a second filter (21 of fig. 1) having an input comprising a non-inverted, the non-inverted output of

the first filter being coupled to the input of the second filter and the output of the first filter (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

However, Coppola does not specifically disclose that the first and second filters are polyphase filters.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Regarding claims 31-35, Coppola discloses a circuit (fig. 1 and fig. 3), comprising: a mixer having an output including a mixed signal output and an inverted mixed signal output (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52); and a filter (21 of fig. 1) having an input including a non-inverted input coupled to the inverted mixed signal output (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

However, Coppola does not specifically disclose that the filter is a polyphase filter.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the

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system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Regarding claim 46, Coppola discloses a circuit (fig. 1 and fig. 3), comprising: a first filter (15 of fig. 1) having an output including a non-inverted output and an inverted input (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52); and a second filter having an input including a non-inverted input coupled to the output of the first polyphase and an input coupled to the non-inverted output of the first polyphase filter (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

However, Coppola does not specifically disclose that the first and second filters are polyphase filters.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter

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with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Regarding claims 54-57, Coppola discloses a circuit (fig. 1 and fig. 3) comprising: mixing means for mixing two signals and outputting a mixed signal and an inverted mixed signal (col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52); and filtering means for notching a particular frequency of the mixed signal; and a means for generating a zero at the particular frequency (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

However, Coppola does not specifically disclose that the first and second filters are polyphase filters.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the



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imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Regarding claim 58, Coppola as modified discloses a circuit (fig. 1 and fig. 3) further comprising a third filtering means for attenuating frequencies above a third frequency of the mixed signal, the third frequency being higher than the particular and second frequencies (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

Regarding claim 59, Coppola discloses a circuit (fig. 1), comprising: first filtering means (14 of fig. 1) for notching a first frequency of a signal using a first polyphase structure (col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52) and second filtering means of the signal using a second filter structure (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65; col. 7, line 26- col. 8, line 13).

However, Coppola does not specifically disclose that the first and second filters are polyphase filters.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially

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removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Regarding claim 60, Coppola as modified discloses a circuit (fig. 1), wherein the first polyphase structure comprises means for generating a first zero at the first frequency, and the second filter structure comprises means for generating a second zero at the second frequency (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

Regarding claim 61, Coppola as modified discloses a circuit (fig. 1), further comprising a third filtering means for attenuating frequencies above a third frequency of the signal, the third frequency being higher than the second frequency (col. 3, line 40- col. 4, line 54).

Regarding claims 62-66, Coppola discloses a method of filtering a signal (fig. 1 and fig. 3) comprising notching a particular frequency of the signal using a filter structure (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

However, Coppola does not specifically disclose that the first and second filters are polyphase filters.

On the other hand, Yu et al, from the same field of endeavor, discloses a signal processor for reducing undesirable signal content that reduces the undesirable signal content by exaggerating the undesirable signal content and then using this exaggerated undesirable signal and adaptive filter means to estimate the undesirable content in the signal and then substantially removing it from the signal. The signal processor includes a signal mapping means for exaggerating the undesirable signal content; and an adaptive filter means for reducing the undesirable signal content using the exaggerated undesirable signal content (figs. 67; col. 2, lines 51-57; col. 3, lines 53-58; col. 4, lines 10-33). Furthermore, the analog circuit receives an input signal and this circuit resolves the input signal into a constituent pair. In addition, Yu shows in figure 8, two polyphase filters that are responsive to produce the correct mapping for the imperfect signals. In addition, the signal mapping circuit provides the correct mapping for the imperfect signals to produce signals and signals suitable for input signals for the adaptive filter with a small and large amount of undesirable signal content, respectively (figs. 8-10, 12-13; col. 5, lines 8-26; col. 5, lines 55- col. 6, line 42). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Yu to the system of Coppola in order to provide a polyphase filter circuit that can produce asymmetric poles as well as zeros.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 20-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Coppola (US Patent No 6236847 B1).

Regarding claim 20, Coppola discloses a notch filter (fig. 1 and fig. 3), comprising: generating means (15 of fig. 1) for generating an output signal comprising a plurality of phases of an input signal (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52); and notching means for notching a particular frequency of the input signal as a function of the phases (fig. 3; col. 4, lines 27-67; col. 6, lines 31-65).

Regarding claim 21, Coppola Stikvoort discloses a notch filter (fig. 1), wherein the input signal comprises a differential signal (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52; col. 7, line 4- col. 8, line 13).); (col. 3, lines 6-32).

Regarding claim 22, Coppola discloses a notch filter (fig. 1), wherein the generating means (15 of fig. 1) further comprises means for generating the output signal with quadrature outputs when the input signal includes the particular frequency (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52; col. 7, line 4- col. 8, line 13).

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Regarding claim 23, Coppola discloses a notch filter (fig. 1 and fig. 3), wherein the notching means comprising means for rejecting the quadrature signal at the particular frequency (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52; col. 7, line 4- col. 8, line 13).

Regarding claim 24, Coppola discloses a notch filter (fig. 1 and fig. 3), wherein the particular frequency is an odd harmonic of the input signal (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52; col. 7, line 4- col. 8, line 13).

Regarding claim 25, Coppola discloses a notch filter (fig. 1 and fig. 3), wherein the particular frequency is a third harmonic of the input signal (col. 7, line 4- col. 8, line 13).

Regarding claim 26, Coppola discloses a method of notching a particular frequency of a signal (fig. 1), comprising: generating (16 of fig. 1) an output signal comprising a plurality of phases of an input signal (22 of fig. 1; col. 2, line 61- col. 3, line 9; col. 3, lines 18-44; col. 4, lines 42-52; col. 7, line 4- col. 8, line 13).).

Regarding claim 27, Coppola discloses a method of notching a particular frequency of a signal (fig. 1 and fig. 3), wherein the generation of the output signal comprises generating the output signal with quadrature outputs when the input signal includes the particular frequency (col. 7, line 4- col. 8, line 13).

Regarding claim 28, Coppola discloses a method of notching a particular frequency of a signal (fig. 1), wherein the notching of the particular frequency comprises rejecting the quadrature signal at the particular frequency (col. 7, line 4- col. 8, line 13).

Regarding claim 29, Coppola as modified discloses a method of notching a particular frequency of a signal (fig. 1), wherein the particular frequency is an odd harmonic of the input signal (col. 7, line 4- col. 8, line 13).

Regarding claim 30, Coppola discloses a method of notching a particular frequency of a signal (fig. 1), wherein the particular frequency is a third harmonic of the input signal (col. 7, line 4- col. 8, line 13).

#### Allowable Subject Matter

5. Claims 2-11, 14-19, 36-45, 47-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### Response to Arguments

6. Applicant's arguments filed on 1-8-2007 have been fully considered but they are not persuasive.

Applicant's representative argues that Coppola teaches away from arrangement of the first polyphase filter and the second polyphase filter.

However, Coppola clearly shows in figure 1, a notch filter path that is established for each notch frequency and includes a bandpass filter and inverter. An input RF signal covering a wide frequency range is applied to all the notch filter paths. Each notch filter path produces an output spectrum that is equal in magnitude and 180.degree out of phase with respect to an undesired frequency spectrum. In addition, the notch filter network also includes a power combiner that combines multiple Rf signals to produce an RF OUT signal. An inverter couples

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the output of the bandpass filter to one port of a summing junction in the power combiner (abstract; col. 4, lines 27-61). Claim 1 does not mention that the first polyphase filter and the second polyphase filter are in parallel or in series. It does not matter if the notch filter paths are in parallel. Coppola shows in figure 3, a notch filter path where the output from the mixer to a bandpass filter comprises two components: the first is the entire spectrum shifted up in frequency by the local oscillator; the other, the spectrum shifted down by the local oscillator frequency (col. 6, lines 28-40).

Applicant's representative also argues that Coppola and Yu do not teach each and every element of claim 1.

However, Yu also shows in figure 8, two polyphase filters that are realized to produce the correct mapping for the imperfect signals (figs. 9-10; col. 5, lines 7-20; col. 5, line 53-col. 6, line 8).

In response to Applicant's argument stating that prior art reference that teaches away from the claimed invention is a significant factor to be considered in determining obviousness.

The examiner still believes that Coppola and Yu teach all the limitations addressed in the above claims.

### Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 571-272-7853. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew D. Anderson can be reached on 571-272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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**PRIMARY EXAMINER**

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